Exhibit A to Second Response to Office Action

CS152 Computer Architecture and Engineering

Lecture 5: Cost and Design

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lecture slides: http://www-inst.eecs.berkeley.edu/~cs152/

Die cost

Wafer cost

Dies per Wafer * Die yield

~ eff Wafer Area Dies per wafer

Die Area

Wafer yield

Die Yield =

Defects_per_unit_area

Die Cost is goes roughly with the cube of the area.

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Jie Yield

,		Raw Die	Raw Dices Per Wafer	Wafer		
wafer diameter	Q	die area (mm²)	mm^2			
	100	144	144 196 256	256	324	400
6"/15cm	139	06	62	4	32	23
8"/20cm	265	177	124	90	89	52
10"/25cm	431	290	206	153	116	06
die yield	23%	19%	16%	16% 12% 11%	11%	10%

typical CMOS process: ? =2, wafer yield=90%, defect density=2lcm2, 4 test sites/wafer

Good Dices Per Wafer (Before Testing!)

		5	
/.E	က	19 11 7	13
) 	S.	7	20
	0	6	32
•		32	
	31	29	96
	6"/15cm	8"/20cm	10"/25cm

typical cost of an 8", 4 metal layers, 0.5um CMOS wafer: ~\$2000

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From "Estimating IC Manufacturing Costs," by Linley Gwennap, Microprocessor Report, August 2, 1993, p. 15

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Other Costs

Packaging cost Testing cost + Die cost IC cost =

Final test yield

Packaging Cost: depends on pins, heat dissipation

Chip	Díe	4	Package		Test &	Total	
	cost	pins	type		Assembly		
386DX	\$4	132	QFP	₹	75	6	
486DX2	\$12	168	PGA	\$17	£ 6	9 C	
PowerPC 601	\$53	304	OFP		7-0	0 1 0 1 0 0	
HP PA 7100	\$73	207	- V) (17¢	1	
		t	4 5	430	\$16	\$124	
DEC Aipna	\$149	431	PGA	\$30	\$23	\$202	
SuperSPARC	\$272	293	PGA	\$20	788	\$326	
Pentium	\$417	273	PGA	\$19	\$37	\$473	

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